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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,410	05/16/2001	Dave MacAdam	5646-52	1980
20792	7590	09/21/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			ELALLAM, AHMED	
PO BOX 37428			ART UNIT	
RALEIGH, NC 27627			PAPER NUMBER	
			2662	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/858,410

Applicant(s)

MACADAM ET AL.

Examiner

AHMED ELALLAM

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>01/21/03, 01/27/03, 05/16/01</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed "first multi-frame data stream received by said switch" as in claims 1, 21, 23, and 27, "plurality of multi-frame data streams received by said switch" as in claims 13, 19 and 30, and "multi-frame data stream received by said switch", must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

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the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1-30, the specification does not describe the frame offset(s) and or delay(s) with respect to a given reference. More specifically, it is not clear to what reference the delay(s) and/or offset(s) are determined.

Regarding claims 16-18, the specification does not adequately describe the claimed limitations of "a first storage device that is disposed internal to said switch and retains frame delay/offset bytes, with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by the switch and the second storage device that is disposed internal to the switch and at least temporarily retains data that identifies presence of an unacceptable frame delay/offset within first storage device". More specifically, the specification doesn't

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describe the retaining of frame **delay/offset** bytes, with each of the frame **offset/delay** bytes **identifying a frame delay or frame offset**, and the second storage device that is disposed internal to the switch and at least temporarily retains data that identifies presence of an unacceptable frame **delay/offset** within first storage device. In addition these limitations have not being described in the body of the specification, they are only stated in the summary.

Regarding claim 17, the specification doesn't adequately describe the feature of "data identifies presence and location of the unacceptable frame delay/offset within said first storage device".

Claims 17 and 18 depend from claim 16, thus they are subject to the same rejections.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, the phrase "a frame delay conversion circuit that converts the frame delays to acceptable frame offsets" is confusing because it is already stated that some frame delays are excessive, a distinction between the excessive frame delays and acceptable frame delays should be made.

Claim 20 depends from claim 19, thus it is subject to the same rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4, 13-16, 23, 27, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, specification pages 1-2 and figure 1-2 in view of Koenig et al, US 6,879,603. Hereinafter referred to as APA and Koenig respectively.

Regarding claim 1, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame offset of a received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch. (Examiner interpreted the combination of both the internal circuitry and external circuitry of prior art (figure 1) as being the claimed an internal frame alignment measurement and programming circuit).

Regarding claims 13 and 30, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame offset of a

received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch. The prior art further discloses using conventional delay limit check circuitry 20 to determine whether the frame delay for a given multi-frame data stream exceeds the rating of the switch, see page 2, lines 10-12. (Claimed determines and then stores an unacceptable frame offset associated with a multi-frame data stream having an offset that exceeds a maximum offset rating of the switch as in claim 13 and determines and then stores an unacceptable frame delay associated with a multi-frame data stream having a delay that exceeds a maximum delay rating of the switch as in claim 13, Examiner interpreted the offset and delays of being similar since the prior art table of figure 2 has a correspondence between the delays and the offsets).

Regarding claim 16, APA discloses time-slot interchange switch comprising:

Conventional table retaining frame delay/offset bytes with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by the switch, see figure 2, specification page 7, lines 30-31 and page 8, line 1, and lines 28-31, page 9, lines 1-4. (Claimed a first storage device that is disposed internal to said switch and retains frame delay/offset bytes, with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by said switch).

Temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1).

Regarding claim 23, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame offset of a received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch. APA further discloses a user reads out the count signal and may use conventional delay limit check circuitry 20 to determine whether the frame delay for a given multi-frame data stream exceeds the rating of the switch, see page 2, lines 9-14.

Regarding claim 27, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame delay of a received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch. The prior art further discloses using conventional delay limit check circuitry 20 to determine whether the frame delay for a given multi-frame data stream exceeds the rating of the switch, see page 2, lines 10-12. (Claimed determines and stores a first frame delay associated with a first multi-frame data stream received by the switch in a frame delay register associated , and at least retain data that identifies presence of an unacceptable frame delay in the internal frame delay register).

As to claims 1, 13, 16, 23, 27 and 30:

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The difference between claims 1, 13, 16, 27 and the prior art is that the temporary register is external to the TSI switch.

However Koenig discloses implementing a TSI within a DSP processor. It would have been obvious to an ordinary person of skill in the art at the time the invention was made to have the external circuitry of the prior art implemented using a single DSP based TSI switch as taught by Koenig so that both internal and external circuitry of prior art can be integrated. The advantage would be the ability to provide flexibility in design and reduction in space of the TSI switch.

Regarding claims 2 and 28, APA discloses a table (figure 2) implemented by internal frame register 18 for retaining data that is accessible by a user, see figure2, page 2, lines 9-14. (Examiner interpreted the function provided by the claimed error code register of being the same as the internal frame offset register 18)

Regarding claims 3 and 4, APA discloses internal frame alignment counter 12 that determine frame delay associated with a first multi-frame data stream, and offset conversion circuit 16 that converts the first delay into a first frame offset.

Regarding claim 14, APA discloses the frame offset register 18 for storing acceptable and unacceptable frame offsets. See figure1 and specification, page 2, lines 9-14.

Regarding claim 15, in addition to the discussed limitation as in claim 14, APA discloses a user access to frame offset from frame offset register 18. See specification, page 2, lines 9-14.

Conclusion


5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Johnson et al, US (4,644,535); Ashi et al, US (5,351,238); Baydar et al, US (5,784,377); Humphrey et al, US (6,246,681); Irwin, US (5,862,136); Dally, US 2001/0033584; Petty, US (6,480,511); Hughes et al, US (6,870,831).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AHMED ELALLAM whose telephone number is (571) 272-3097. The examiner can normally be reached on 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kizou Hassan can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AHMED ELALLAM
Examiner
Art Unit 2662
September 14, 2005


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